CLAIMS

I claim:

1. A method for timestamping events in a primary event stream, the method comprising:

receiving the primary event stream;

distributing events in the primary event stream among a plurality of secondary event streams; and

timestamping events in each of the secondary event streams.

2. The method of Claim 1 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

3. The method of Claim 1 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

4. The method of Claim 1 wherein the primary event stream is a differential signal.

5. The method of Claim 1 wherein the secondary event streams are differential signals.

6. The method of Claim 1 wherein distributing comprises selectively enabling a plurality of gates such that a first event in the primary event stream is passes

through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

7. The method of Claim 1 wherein distributing comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

8. The method of Claim 1 wherein distributing comprises:

distributing rising edge events in the primary event stream among a first plurality of secondary event streams; and

distributing falling edge events in the primary event stream among a second plurality of secondary event streams.

9. The method of Claim 1 further comprising:

registering the events in each of the secondary event streams.

10. A circuit for timestamping events in a primary event stream, the circuit comprising:

an event stream distributor coupled to receive the primary event stream; and

a plurality of timestamp circuits, each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor.

11. The circuit of Claim 10 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

12. The circuit of Claim 10 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

13. The circuit of Claim 10 wherein the primary event stream is a differential signal.

14. The circuit of Claim 10 wherein the secondary event streams are differential signals.

15. The circuit of Claim 10 wherein the event stream distributor comprises:

a first counter coupled to receive the primary event stream; and

a first plurality of gates coupled to the first counter.

16. The circuit of Claim 15 wherein the first counter is a Johnson counter.

17. The circuit of Claim 15 wherein the first counter is an N-bit counter.

18. The circuit of Claim 15 further comprising:

a second counter coupled to receive the primary event stream; and

a second plurality of gates coupled to the second counter.

19. The circuit of Claim 10 further comprising:

a plurality of registers, each register operable to register events of one or more secondary event streams.

20. A method for timestamping events in a primary event stream, the method comprising:

receiving the primary event stream;

distributing rising edge events in the primary event stream among a first plurality of secondary event streams;

recording an arrival time of each event in the first plurality of secondary event streams with respect to a reference clock;

distributing falling edge events in the primary event stream among a second plurality of secondary event streams; and

recording an arrival time of each event in the second plurality of secondary event streams with respect to the reference clock.

21. The method of Claim 20 wherein an event rate in each secondary event stream of the first plurality and the second plurality of secondary event streams is lower than an event rate in the primary event stream.

22. The method of Claim 20 wherein the primary event stream is a differential signal.

23. The method of Claim 20 wherein each secondary event stream of the first plurality and the second plurality of secondary event streams are differential signals.

24. The method of Claim 20 wherein distributing rising edge events comprises selectively enabling a first plurality of gates and distributing falling edge events comprises selectively enabling a second plurality of gates.

25. The method of Claim 20 wherein distributing rising edge events comprises selectively enabling a first plurality of gates using a first counter that is clocked by the primary event stream and distributing falling edge events comprises selectively enabling a second plurality of gates using a second counter that is clocked by the primary event stream.

26. A circuit for timestamping events in a signal, the circuit comprising:

a first counter coupled to receive the signal; and

a first plurality of gates, each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter.

27. The circuit of Claim 26 wherein the first plurality of gates are AND gates.

28. The circuit of Claim 26 wherein the signal is a differential signal.

29. The circuit of Claim 26 wherein the signal is a single-ended signal.

30. The circuit of Claim 26 wherein the first counter is a Johnson counter.

31. The circuit of Claim 26 wherein the first counter is an N-bit counter.

32. The circuit of Claim 26 further comprising:

a second counter coupled to receive the primary event stream; and

a second plurality of gates, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the second counter.

33. A circuit comprising:

a buffer having an input coupled to receive an input signal;

a first counter having an input coupled to receive a first output signal from the buffer; and

a first plurality of AND gates, each AND gate having a first input coupled to receive the first output signal from the buffer and a second input coupled to receive a respective output signal from the first counter.

34. The circuit of Claim 33 wherein the buffer is a differential buffer.

35. The circuit of Claim 33 wherein the first counter is a Johnson counter.

36. The circuit of Claim 33 wherein the first counter is an N-bit counter.

37. The circuit of Claim 33 wherein the first output signal from the buffer includes a plurality of rising edges and each rising edge is used to clock the first counter.

38. The circuit of Claim 33 wherein the first output signal from the buffer includes a plurality of falling edges and each falling edge is used to clock the first counter.

39. The circuit of Claim 33 further comprising:

a second counter having an input coupled to receive a second output signal from the buffer; and

a second plurality of AND gates, each AND gate having a first input coupled to receive the second output signal from the buffer and a second input coupled to receive a respective output signal from the second counter.

40. A method comprising:

receiving a signal having events at N gates;

selectively enabling each of the N gates such that a first event passes through a first gate, a second event passes through a second gate, a third event passes through a third gate, and so on, until an Nth event passes through a Nth gate; and

recording an arrival time of each event with respect to a reference clock

41. The method of Claim 40 wherein selectively enabling each of the N gates comprises:

clocking a counter using the signal; and

selectively enabling each of the N gates using a plurality of output signals generated by the counter.

42. The method of Claim 40 wherein the gates are AND gates.